Workshop Program
Krakow, Poland, February 15, 2010

[11:00-12:30] S1: Design and Analysis
Session Chair: Sabri Pllana, University of Vienna, Austria

- Keynote Address “MPSoC Design Technologies for Wireless Multimedia Terminals.”
  Rainer Leupers, RWTH Aachen University, Germany

- “Scalability Analysis of Progressive Alignment in a Multicore.”
  Sebastian Isaza, Friman Sanchez, Georgi Gaydadjiev, Alex Ramirez, Mateo Valero

- “Simulation and Performance Analysis of Multi-Core Thread Scheduling and Migration Algorithms.”
  Fadi Sibai

[12:30-14:00] LUNCH BREAK

[14:00-15:30] S2: Programmability
Session Chair: Fatos Xhafa, Technical University of Catalonia, Spain

- “Automatic Offloading of C++ for the Cell BE Processor: a Case Study Using Offload.”
  Alastair Donaldson, Uwe Dolinsky, Andrew Richards, George Russell

- “A Parallel Programming Framework for Multi-Core DNA Sequence Alignment.”
  Tiago Almeida, Nuno Roma

- “A multidimensional array slicing DSL for Stream Programming.”
  Pablo de Oliveira Castro, Stéphane Louise, Denis Barthou

- “Study of Variations of Native Program Execution Times on Multi-Core Architectures.”
  Abdelhafid Mazouz, Sid-Ahmed-Ali Touati, Denis Barthou

[15:30-16:00] COFFEE BREAK

[16:00-17:30] S3: Resource Usage Optimization and Interconnection Networks
Session Chair: Sabri Pllana, University of Vienna, Austria

- “A Simple Improvement of the Work-Stealing Scheduling Algorithm.”
  Zeljko Vrba, Paal Halvorsen, Carsten Griwodz

- “Threaded Dynamic Memory Management in Many-Core Processors.”
  Edward Herrmann, Philip Wilsey

- “A Fuzzy Logic Reconfiguration Engine for Symmetric Chip Multiprocessors.”
  Muhammad Yasir Qadri, Klaus McDonald Maier

- “Low Diameter Unicast On-Chip Interconnection Networks for Many-Core Embedded Systems.”
  Fadi Sibai